Claims

[c1] What is claimed is:

1. A method of fabricating a vertical metal-oxide semiconductor (MOS) transistor, the method comprising:

providing a silicon substrate;

forming a gate mask on the silicon substrate;

etching region of the silicon substrate not covered by the gate mask to a predetermined depth;

forming a silicon oxide layer on the region of the silicon substrate not covered by the gate mask;

forming, in order, a poly silicon germanium ($Si_{1-x}Ge_x$, x = 0.05~~1.0) layer and a poly silicon layer, respectively, on the a surface of the silicon substrate;

performing a first etching back process to form a first spacer consisting of the poly silicon layer, the poly silicon germanium layer and the silicon oxide layer on the region of the silicon substrate below the gate mask;

removing the gate mask;

performing a selective etching process to remove portions of both the poly silicon germanium layer and the silicon oxide layer;

performing a doping process to form lightly doped drains (LDD) of the vertical MOS transistor; and

performing a first ion implantation process to form a drain and a source of the vertical MOS transistor.

[c2]

2. The method of claim 1 wherein a method of forming the gate mask comprises:

forming a patterned first sacrificial layer on the surface of the silicon substrate;

forming a second sacrificial layer on the silicon substrate to cover the first sacrificial layer;

performing a second etching back process on the second sacrificial layer to form at least one second spacer consisting of the second sacrificial layer on the side wall of the first sacrificial layer, the second spacer functioning as the gate mask; and

removing the first sacrificial layer.

[c3] 3. The method of claim 2 wherein the first sacrificial layer comprises silicon oxide compounds, and the second sacrificial layer comprises silicon nitride compounds.

[c4] 4. The method of claim 1 wherein the doping process comprises a plasma doping process.

[c5] 5. The method of claim 1 wherein the method further comprises a second ion implantation process to adjust a threshold voltage (V_t) of the vertical MOS transistor.

[c6] 6. A method of fabricating a vertical metal-oxide semiconductor (MOS) transistor, the method comprising:
providing a silicon substrate;
forming a gate mask on the silicon substrate;
etching region of the silicon substrate not covered by the gate mask to a predetermined depth;
forming a silicon oxide layer on the region of the silicon substrate not covered by the gate mask;
forming a first conductive layer and a second conductive layer, respectively, on the a surface of the silicon substrate;
performing a first etching back process to form a first spacer consisting of the second conductive layer, the first conductive layer and the silicon oxide layer on the region of the silicon substrate below the gate mask;
removing the gate mask;
performing a selective etching process to remove portions of both the first conductive layer and the silicon oxide layer;
performing a doping process to form lightly doped drains (LDD) of the vertical MOS transistor; and
performing a first ion implantation process to form a drain and a source of the vertical MOS transistor.

[c7] 7. The method of claim 6 wherein a method of forming the gate mask comprises:

forming a patterned first sacrificial layer on the surface of the silicon substrate;

forming a second sacrificial layer on the silicon substrate to cover the first sacrificial layer;

performing a second etching back process on the second sacrificial layer to form at least one second spacer consisting of the second sacrificial layer on the side wall of the first sacrificial layer, the second spacer functioning as the gate mask; and

removing the first sacrificial layer.

[c8] 8. The method of claim 7 wherein the first sacrificial layer comprises silicon oxide compounds, and the second sacrificial layer comprises silicon nitride compounds.

[c9] 9. The method of claim 6 wherein the doping process comprises a plasma doping process.

[c10] 10. The method of claim 6 wherein the first conductive layer comprises poly silicon germanium and the second conductive layer comprises doped poly silicon.

[c11] 11. The method of claim 6 wherein the first conductive layer comprises poly silicon germanium and the second conductive layer comprises undoped poly silicon.

[c12] 12. The method of claim 6 wherein the first conductive layer comprises amorphous silicon and the second conductive layer comprises poly silicon.

[c13] 13. The method of claim 6 wherein after the region of the silicon substrate not covered by the gate mask is etched to the predetermined depth, the method further comprises a second ion implantation process to adjust a threshold voltage (V_t) of the vertical MOS transistor.